

Appln. No. 09/832,435
Amdt. dated May 22, 2006
In Reply to Office Action of Feb. 22, 2006

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an error detection module for determining, based upon said syndromes, a number of errors within said codeword; and

a comparator for comparing said number of errors to a threshold value, said codeword corresponding to a valid codeword when said number of errors is less than said threshold value.

18. (Currently Amended) The codeword synchronization module of claim 4 ~~3~~ further including an error correction circuit for carrying out an error correction operation on said codeword using error correction information provided by said plurality of phase synchronizers.

19. (Original) The method of codeword synchronization of claim 9 further including carrying out an error correction operation on said codeword on the basis of an error location polynomial derived from said first syndromes.

20. (Previously Presented) A codeword synchronization system comprising:
a sampling arrangement for generating N bitstreams in response to a received data stream, where N is an integer;
a set of N codeword synchronization modules, each of said N codeword synchronization modules providing a plurality of codeword error signals indicative of a number of errors associated with a corresponding plurality of potential phases of one of said N bitstreams; and
a phase selection module for identifying one of said codeword error signals as being indicative of a lowest number of errors.

21. (Original) The codeword synchronization system of claim 20 wherein a first of said set of N codeword synchronization modules includes:

an input shift register for receiving a first of said N bitstreams, said first of said N bitstreams containing a codeword, and

a plurality of syndrome computing modules, each of said syndrome computing modules computing syndromes being associated with a different one of said plurality of potential phases of said codeword.

22. (Previously Presented) The codeword synchronization system of claim 21 wherein said first of said set of N codeword synchronization modules further includes a plurality of error

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detection modules, each of said error detection modules determining a number of errors associated with a corresponding one said plurality of potential phases of said codeword using the syndromes produced by an associated one of said plurality of syndrome computing modules.

23. (Original) The codeword synchronization system of claim 20 wherein said sampling arrangement includes:

a sampling circuit; and

a clock coupled to said sampling circuit, said clock being operative at N times a data rate of said received data stream.

24. (Previously Presented) The codeword synchronization system of claim 23 wherein said sampling arrangement further includes a demultiplexer having an input port connected to said sampling circuit and a set of N output ports connected to said set of N codeword synchronization modules.